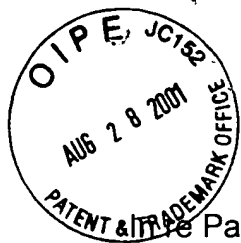


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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
ATTY. DOCKET NO. 13691

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Patent Application of Richard S. NORMAN et al.

Serial No. 09/870,767

Group Art Unit: 2661

Filed: June 1, 2001

Examiner:

For: **CELL-BASED SWITCH FABRIC WITH INTER-CELL CONTROL  
FOR REGULATING PACKET FLOW**

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

This Information Disclosure Statement is being filed in the manner prescribed by 37 CFR 1.97(b) - (d) to satisfy the duty under 37 CFR 1.56 to disclose to the Office information, known to individuals associated with the filing and prosecution of the subject application, which is material to the examination of the application.

In accordance with 37 CFR 1.97(g) and (h), this statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 CFR 1.56(b).

This information disclosure statement is being filed within three months of the filing date of a national application, within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; or before the mailing date of a first official action on the merits and therefore applicant respectfully requests consideration under 37 CFR 1.97(b).

In compliance with 37 CFR 1.98(a)(1), a list of all patents, publications or other information submitted for consideration by the Office is hereby provided by way of the attached Form PTO 1449.

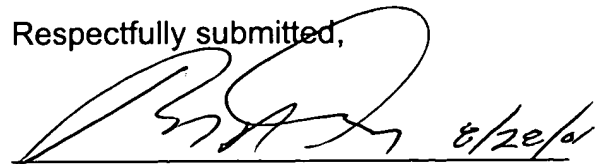
In compliance with 37 CFR 1.98(a)(2), also enclosed is a legible copy of:

- i) each United States and foreign patent;
- ii) each publication or that portion which caused it to be listed; and
- iii) all other information or that portion which caused it to be listed, excluding any copies of a United States patent application.

It is respectfully requested that the information be expressly considered by the Examiner and that the references be made of record and appear among the "References Cited" on any patent to issue therefrom.

The Patent Office is hereby authorized to charge any deficiency, or credit any overpayment in fees to Deposit Account Number

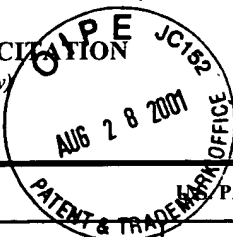
Respectfully submitted,



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Encls: Form PTO-1449  
All references listed on Form PTO-1449  
Acknowledgement Card

**INFORMATION DISCLOSURE CITATION**  
(Use several sheets if necessary)



Docket Number (Optional)

13691

Application Number

09/870,767

Applicant(s)

Richard NORMAN et al.

Filing Date

June 1, 2001

Group Art Unit

2661

**PATENT DOCUMENTS**

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	1.	U.S. 4,849,751	18/07/1989	Barber et al.			
	2.	U.S. 5,072,366	10/12/1991	Simcoe			
	3.	U.S. 4,955,020	04/09/1990	Stone et al.			

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**FOREIGN PATENT DOCUMENTS**

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

**OTHER DOCUMENTS** (Including Author, Title, Date, Pertinent Pages, Etc.)

	4.	French, R., Architectural Consideration for Internet Routers; retrieved from the internet guideline in file; Internet URL www.cise.ufl.edu/ rfrench, accessed July 23, 2001;
	5.	Joseph Desposito; Router-On-A-Chip Manages Network Traffic with Wire-Speed QoS; Electronic Design; May 1, 2000; pp 64-65-66;

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE CITATION</b> (Use several sheets if necessary)		Docket Number (Optional) <b>13691</b>		Application Number <b>09/870,767</b>	
		Applicant(s) <b>Richard NORMAN et al.</b>			
		Filing Date <b>June 1, 2001</b>		Group Art Unit <b>2661</b>	
*EXAMINER INITIAL		OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, Etc.)			
		6. Werner Bux et al.; Technologies and Building Blocks for Fast Packet Forwarding; IEEE Communications Magazine; January 2001; pp. 70-77.			
		7. Minagawa, N. et al. ; Dept. of Comput. Scil, University of Electro-Commun. Tokyo, Japan; Implementation of a network switch on chips;(Abstract) Communications, vol. 13, no. 1; retrieved on March 16, 2001 from INSPEC database.			
		8. Saturn: a terabit packet switch using dual round-robin; (abstract) Globecom'00 - IEEE, Global Telecommunications Conference; Dept. of Electr. Eng. Polytech, Univ.of Brooklyn, NY, U.S.A.; retrieved on June 4, 2001 from INSPEC database.			
		9. Nanette J. Boden et al.; Myrinet - Gigabit-per-Second Local-Area Network [on line]; November 16, 1994 Myricom, Inc.; Internet URL <a href="http://www.myrinet.com/research/publications/Hot.ps">http://www.myrinet.com/research/publications/Hot.ps</a> ; retrieved on March 14, 2001;			
		10. Vitesse Semiconductor Corporation [on line] ; Datasheet VSC880; January 5, 2001; pp. 1-20; retrieved on July 23, 2001; Internet URL <a href="http://www.vitesse.com/products/documents.cfm?family=document-id=180">www.vitesse.com/products/documents.cfm?family=document-id=180</a> ;			
		11. Vitesse Semiconductor Corporation [on line] ; Datasheet VSC870; June 29, 2001; pp. 1-40; retrieved July 23, 2001; Internet URL <a href="http://www.vitesse.com">www.vitesse.com</a>			
		12. A New Architecture for Switch and Router Design; PMC-Sierra Inc.; December 22, 1999; Internet URL <a href="http://www.pmc-sierra.com/pressRoom/pht/1cs_wp.pdf">http://www.pmc-sierra.com/pressRoom/pht/1cs_wp.pdf</a> retrieved on July 4, 2001; pp. 1-8;			
		13. Network Processor Designs for Next-Generation Networking Equipment [on line] ; EZ Chip Technologies; Internet URL <a href="http://www.ezchip.com/images/pdfs/etchip_white_paper.pdf">http://www.ezchip.com/images/pdfs/etchip_white_paper.pdf</a> ; retrieved on July 4, 2001; December 1999; pp.1-4.			
		14. Cyrel Minkenberg et al. A combined Input and Output Queued Packet-Switched System Based on Prisma Switch-on-a-Chip Technology; Scalable High-Speed Switches/Routers with QoS Support; IBM Research, Zurich Research Laboratory; IEEE Communications Magazine; December 2000; pp 70-84;			
		15. Werner Bux et al.; Technologies and Building Blocks for Fast Packet Forwarding; Telecommunications Networking at the Start of the 21st Century; IEEE Communications Magazine; January 2001; pp 70-77;			
		16. Child, J.; Bus-switching chip busts bandwidth barrier [on line] ; Internet URL <a href="http://www.computer-design.com/editorial/1995/06/directions/bus.html">http://www.computer-design.com/editorial/1995/06/directions/bus.html</a> ; retrieved on March 15, 2001.			
		17. PSID - Based Communications Switching [on line] ; December 1997; Internet URL <a href="http://www.icube.com/commsw.pdf">http://www.icube.com/commsw.pdf</a> ; retrieved on March 15, 2001; pp 1-14			
EXAMINER		DATE CONSIDERED			
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